150V N-Ch Power MOSFET

V_{DS}		150	V
$R_{DS(on),typ}$	V_{GS}=10V	7.5	m
$R_{DS(on),typ}$	V_{GS}=4.5V	8.8	m
$I_{D\ (Sillicon\ Limited)}$		87	A
$I_{D\ (Package\ Limited)}$		60	A

Part Number	Package	Marking
HGN088N15SL	DFN5*6	GN088N15SL

Absolute Maximum Ratings at T_j

Parameter		Conditions	Value	Unit
		T_C	55	A
Continuous Drain Current (Package Limitec		T_C	60	
Drain to Source Voltage	V_{DS}	-		
Gate to Source Voltage	V_{GS}	-	20	
Pulsed Drain Current	I_{DM}			
Avalanche Energy, Single Pulse	E_{AS}	L=0.4mH, T_C		
Operating and Storage Temperature	T_J, T_{stg}	-		

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	R_{JA}	55	
Thermal Resistance Junction-Case	R_{JC}	0.9	

Electrical Characteristics at T_j

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	150	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	1	2	3	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=150V, T_j	-	-	1	A
		V_{GS}=0V, V_{DS}=150V, T_j	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS} s99 $_{DS}$=0V	-	-	100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	7.5	8.8	m
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=20A	-	8.8	11	m
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	85	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	0.95	-	

Dynamic Characteristics

Input Capacitance			-	4758	-	
					-	pF
Total Gate Charge	Q_g(10V)					
Gate to Source Charge	Q_{gs}					

Fig 1. Typical Output Characteristics

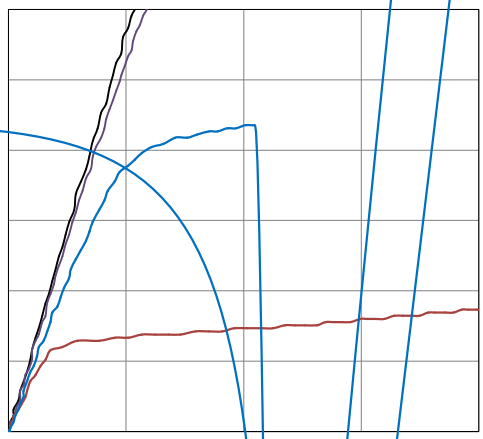


Figure 2. On-Resistance vs. Gate-Source Voltage

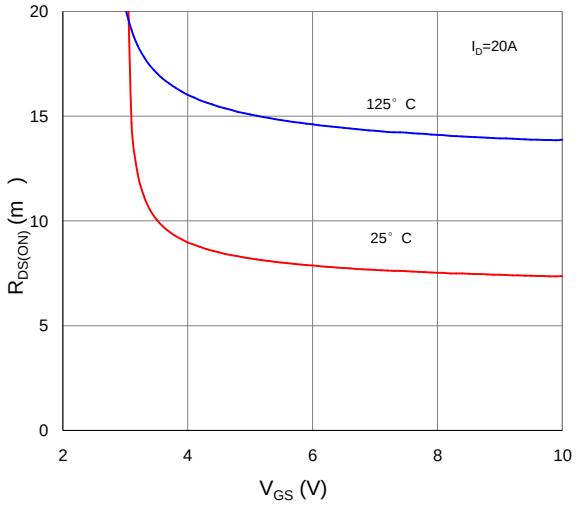


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

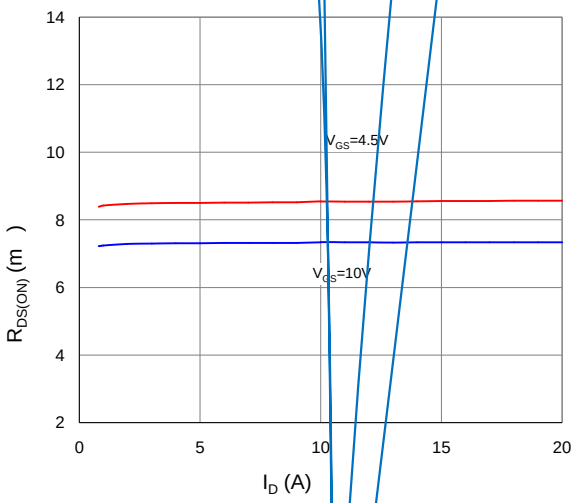


Figure 4. Normalized On-Resistance vs. Junction Temperature

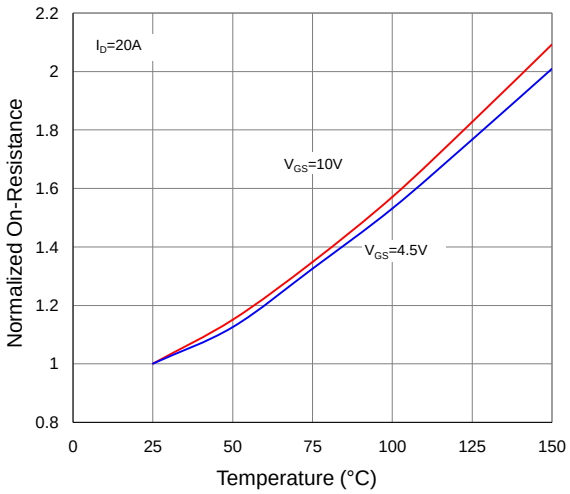


Figure 5. Typical Transfer Characteristics

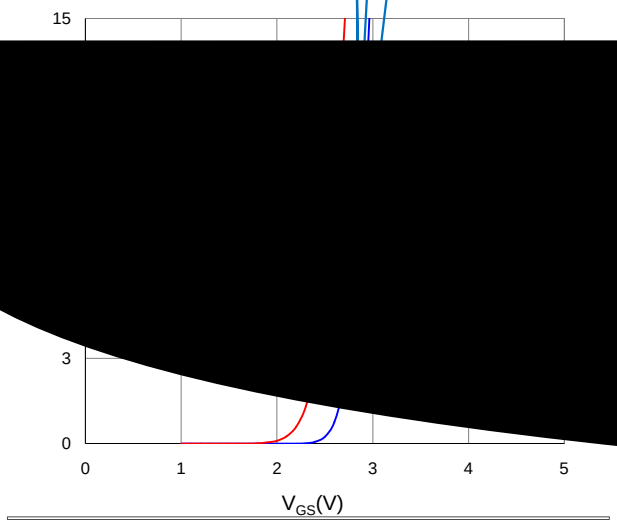


Figure 6. Typical Source-Drain Diode Forward Voltage

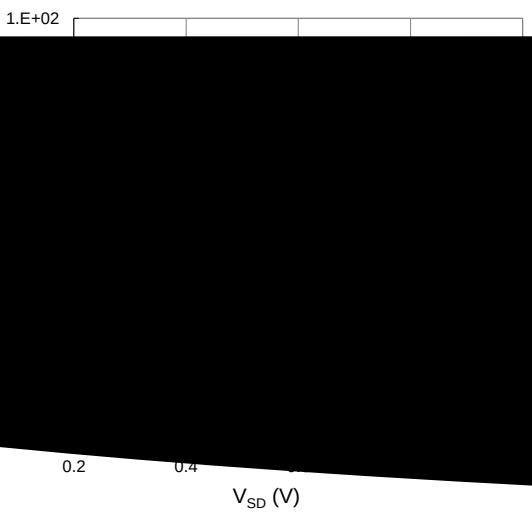


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

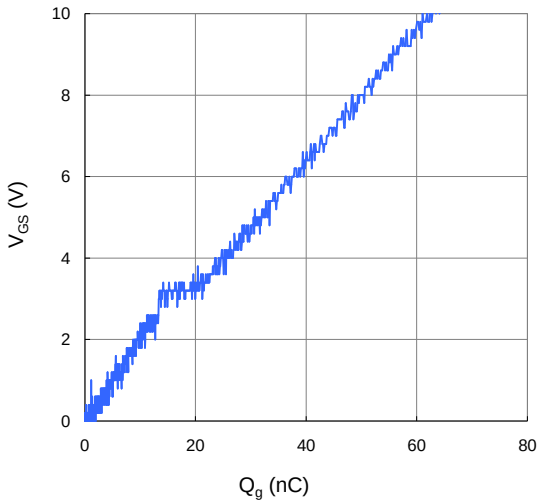


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

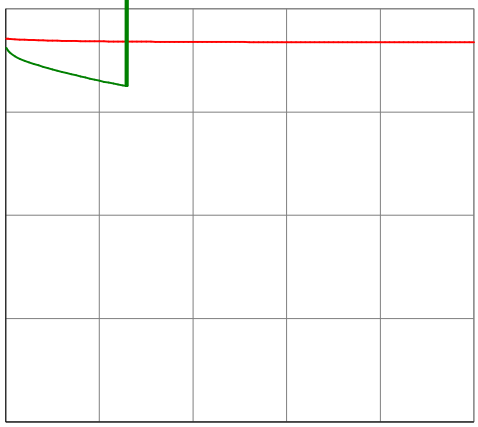
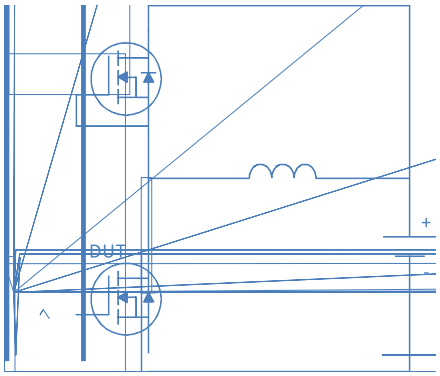


Figure 9. Maximum Safe Operating Area

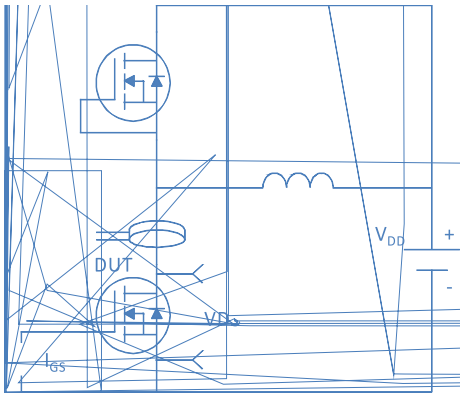
Figure 10. Maximun Drain Current vs. Case Temperature

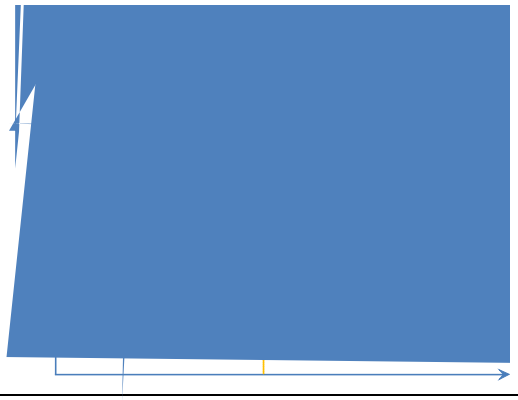
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

Inductive switching Test

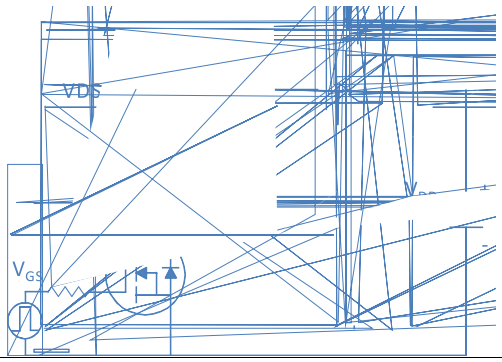


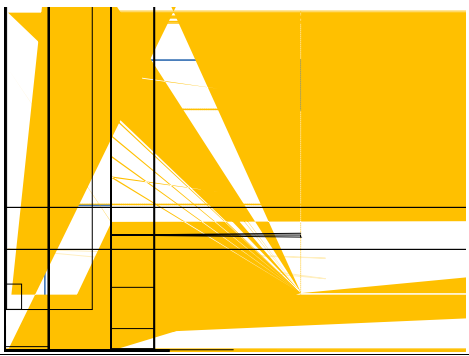
Gate Charge Test



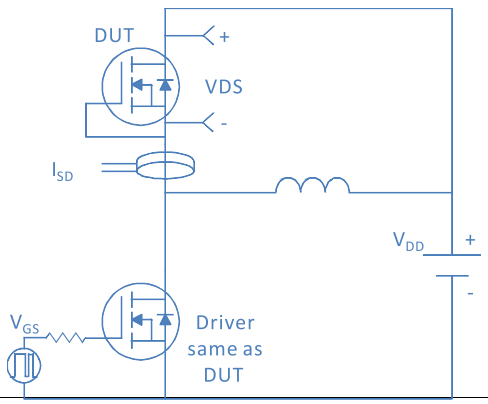


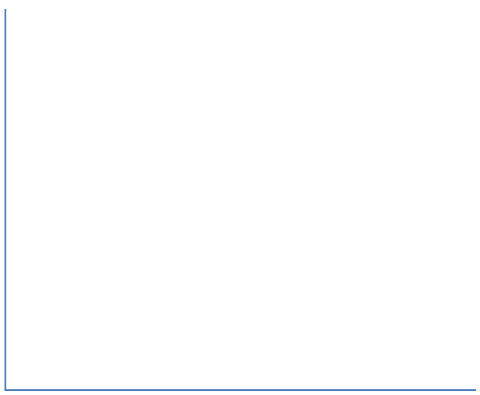
Uclamped Inductive Switching (UIS) Test





Diode Recovery Test





Package Outline

DFN5x6_P, 8 Leads